DIGITAL INDUSTRIES SOFTWARE

Z-planner Enterprise

PCB Stackup Planning

Benefits

- Automatically qualify fabricators' stackups to ensure that they comply with design and manufacturing requirements.
- Stackup-design standardization saves time and reinforces best practices
- Select the best laminate system for each design with comprehensive CCL material decision support
- Maximize profitability with cost management and value engineering (VE)
- Integrate stackup data with signal integrity simulators early to ensure valid simulations

Overview

The stackup forms the foundation of a PCB, its design interacts with every high-speed signal on a PCB. That's why it is important to take control of your stackup with Z-planner Enterprise. Z-planner Enterprise is a field-solver based PCB stackup planning and materials selection software that gives you complete control over not only the design of a stackup, but also the fabrication of the stackup.

Z-planner Enterprise includes an accurate field solver, a loss-planning environment, and a complete dielectric materials library – all seamlessly interfaced to the most popular signal-integrity software. With ever-increasing edge rates, accurate loss and impedance calculations with actual dielectric materials data is imperative to getting the stackup right the first time.

Z-planner Enterprise Includes:

- Everything necessary for automated design and management of PCB stackups and laminate selection, including a stackup wizard
- Interfaces to common PCB layout and signal-integrity design flows
- DFM and DFSI design-rule management and checking

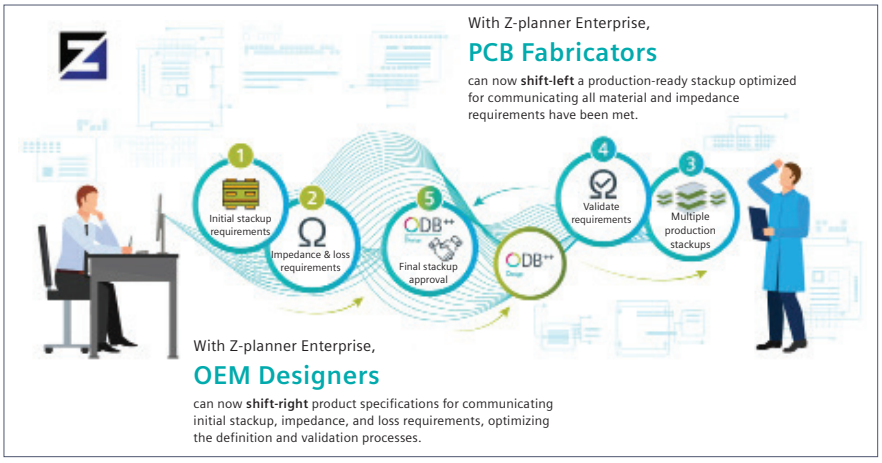
Features

- Integrated HyperLynx field solver
- Unlimited layer count and impedance groups
- Supports rigid and rigid-flex technology
- Advanced stackup wizard
- Glass awareness and Glass-Weave Skew mitigation
- Compare fabricator stackups with detailed manufacturing properties
- Stackup cross-section simulation including microstrips, buried microstrips, striplines and coplanar waveguides
- Via editor to determine manufacturing sequence

SI	Improved simulation accuracy	• Actual laminate Dk/Df values • Impedance planning • % Cu/Prepreg thicknesses • Los planning • Glass-weave skew • CCL copper roughness • Fab process roughness • Etch effects/orientation • Improved crosstalk modeling • Coplanar waveguide simulation
CAD	Integrated with your PCB design flow	• 100% digital design flow • Automated stackup creation • HyperLynx import/export • IPC-2581 import/export • ODB++ import/export • Xpedition import/export • Excel import/export
NPI	Comprehensive material management	• Cost control and value engineering (VE) • Automated DFx rule checking • MML/Library management • CCL material decision support • Construction-use management

- Compare multiple fab stackups
- Consistent repository and methodology
- Enforce DFx rules

- Unlimited stackup-layer support – including automated calculation of width/spacing for target impedances
- HyperLynx field solver – simulating dielectric and copper losses
- Z-solver – detailed cross-section analysis, including S-parameter export
- Stackup viewer – display and output board thickness, via connectivity and impedance tables for rigid and rigid-flex boards.



Z-planner Enterprise integrates seamlessly into the typical PCB design flow. From pre-layout signal integrity exploration, to post-layout stackup verification across multiple PCB fabricators. Z-planner manages the entire process, including revision control and interoperability with PCB layout and signal-integrity software.

Fully integrated into the PCB design flow

Z-planner Enterprise optimizes the process of defining and documenting stackup requirements early in the design process, ensuring that pre-layout signal-integrity simulations are based on the most-accurate laminate-data available using a consistent stackup-design methodology. Stackup validation across multiple PCB fabricators is automated and final stackups can easily be exported for post-layout signal-integrity signoff.

New-product introduction (NPI) engineers send the Excel version of the specified stackup from Z-planner Enterprise to each PCB fabricator (typically three or more fabricators, depending on production volumes).

Z-planner Enterprise benefits the entire team

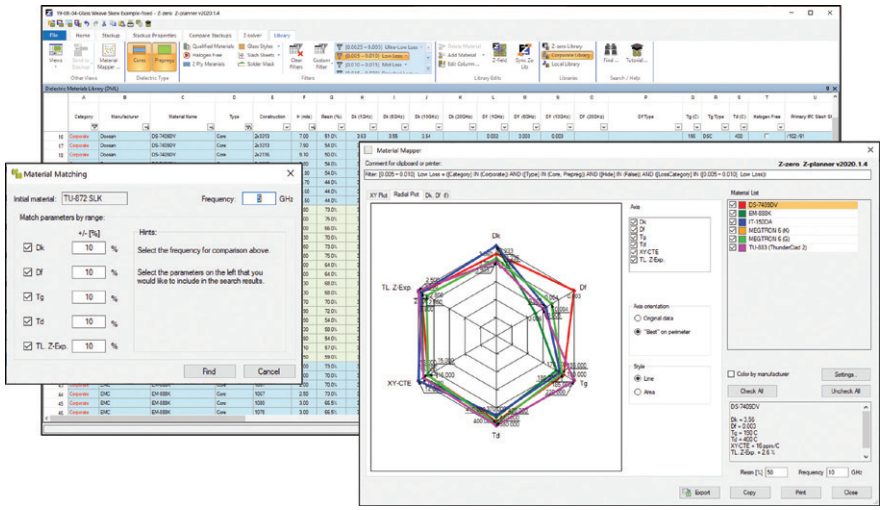
PCB fabricators respond with their unique, process-dependent and proprietary implementations of the stackup spec for import into Z-planner, followed by DFM (design for manufacturing) and DFSI (design for signal integrity) checks across 33 different stackup-design parameters.

PCB laminate library

Z-planner Enterprise contains an ever-expanding dielectric materials library providing detailed specifications on dielectric-materials data from popular manufacturers AGC-Nelco, Rogers, Dupont, Showa Denko, EMC, Doosan, ITEQ, Nanya, Panasonic, Shengyi, TUC, and Ventec.

The dielectric materials library provides qualified PCB-laminate materials from 180 laminate families that can be inserted directly into the field solver for instant material comparison and qualification. Complete material information is available for each selection, including frequency-dependent Dk and Df values for thousands of core and prepreg combinations right out of the box. In addition, the materials library contains resin content, glass style, and pressed prepreg thickness – all critical parameters for getting high speed stackups right the first time.

Built-in and customizable filters allow for the quick selection of any electrical or mechanical parameters, such as halogen-free materials, dual-ply cores, and even a complete set of IPC-4101 slash sheets.



The dielectric materials library interfaces directly with the Z-solver, the integrated field solver, allowing users to directly compare Dk and Df measurements from laminates from 1-20 GHz.

The Material Matching™ feature allows for quick redesigns of the stackup based on selected material parameters. The Material MapperTM provides comprehensive graphical plots including Dk, Df, Tg, Td, z-CTE and x-y CTE.

With library data from thirteen leading laminate manufacturers containing over 180 materials, you can be sure that the specifications of the laminate you choose will be available in the Dielectric Materials Library.

Design reuse

Z-planner Enterprise allows for proven stackups to be reused, saving time and improving the quality of those projects. Structure shared corporate libraries of reusable stackups, organized by layer count, signal/power/ground assignments, impedance classes, board thickness, and PCB dielectrics. Once a stackup has been proven, there is considerable time and cost-saving with reuse.

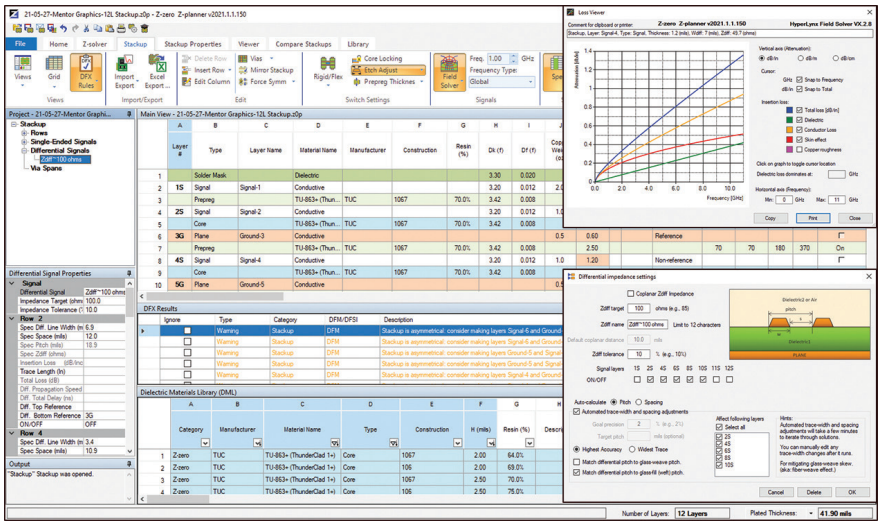
Hardware-design teams

Hardware-design teams can use Z-planner Enterprise for automated design. They can design a stackup using impedance analysis and loss planning with actual laminates, including frequency-dependent dielectric constants and loss tangents, as well as copper roughness from the dielectric library.

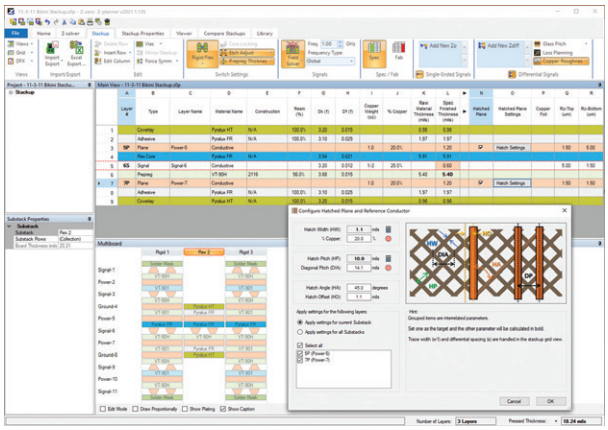
NPI teams

NPI teams use Z-planner Enterprise for automated comparisons between the spec stackup and the fabricators' stackups, including impedance requirements, board thickness, trace widths and pitch.

Detailed DFM and DFSI (Design for Signal Integrity) checks can also be applied to multiple fabricator stackups, ensuring consistent quality and design margins.



Hardware designers can see frequency-dependent Dk and Df for major high-speed PCB laminates out of the box.



Z-planner Enterprise provides detailed stackup layout information such as comprehensive hatched plane designing, glass weave skew mitigation, and, producing higher quality stackup designs faster.

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For additional numbers, click here.

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